CLAIMS

1. An electrostatic discharge (ESD) protection circuit comprising:

a resistor; and

an insulated gate bipolar transistor (IGBT) comprising:

a first well region, wherein the IGBT collector is within the first well region;

a second well region, wherein the IGBT emitter is within the second well region;

a third well region between the first well region and the second well region, the third well region being coupled to the second well region by the resistor;

an insulating region between the IGBT collector and the IGBT emitter and over the third well region; and

a gate electrode over the third well region, the gate electrode being completely separated from the third well region by the insulating region.

2. The ESD protection circuit of Claim 1, wherein the IGBT further comprises:

an emitter electrode in contact with the IGBT emitter; and

at least one isolation structure connecting the third well region and the emitter electrode, wherein the at least one isolation structure and the third well region have a first conductivity type, and wherein the resistor comprises the at least one isolation structure.

3. The ESD protection circuit of Claim 2, wherein the at least one isolation structure includes a heavily doped portion having the first conductivity type, the heavily doped portion being in contact with the emitter electrode, and

wherein the heavily doped portion is located remotely from the IGBT emitter.

4. The ESD protection circuit of Claim 3, wherein the first well region, the second well region, and the IGBT emitter have n-type conductivity, and

wherein the IGBT collector, the third well region, and the at least one isolation structure have p-type conductivity.

5. The ESD protection circuit of Claim 1, wherein the IGBT further comprises a punch through reduction region forming a first butting junction with the insulating region and a second butting junction with the IGBT collector, wherein the IGBT collector has the first conductivity type and the punch through reduction region has a second conductivity type.

6. The ESD protection circuit of Claim 1, wherein the first well region comprises a heavily doped buffer region that forms a butting junction with the insulating region, and wherein the IGBT collector is formed within the heavily doped buffer region.

7. The ESD protection circuit of Claim 1, wherein the IGBT further comprises:

a first emitter electrode in contact with the IGBT emitter;

a second emitter electrode connected to the first emitter electrode by the resistor; and

at least one isolation structure connecting the third well region and the second emitter electrode, wherein the at least one isolation structure and the third well region have a first conductivity type.

8. The ESD protection circuit of Claim 7, wherein the at least one isolation structure includes a first heavily doped portion, the first heavily doped portion having the first conductivity type, and the first heavily doped portion being in contact with the second emitter electrode.

9. An integrated circuit (IC) comprising:

a contact pad; and

a transistor coupled between the contact pad and a ground potential, wherein the transistor comprises:

a collector electrode;

a first emitter electrode;

a parasitic pnp transistor; and

a parasitic npn transistor coupled to the parasitic pnp transistor to form a parasitic thyristor between the collector electrode and the first emitter electrode;

a second emitter electrode coupled to a base of the parasitic npn transistor; and

a resistor connecting a base of the parasitic npn transistor to an emitter of the parasitic npn transistor.

10. The IC of Claim 9, wherein the parasitic pnp transistor comprises a p-well, a first n-well forming a first butting junction with the p-well, and a p-type collector region formed in the first n-well, the p-type collector region being in contact with the collector electrode, and

wherein the parasitic npn transistor comprises the first n-well, the p-well, and a second n-well forming a second butting junction with the p-well, the second n-well including a heavily doped n-type emitter region in contact with the first emitter electrode.

11. The IC of Claim 10, wherein the transistor further comprises:

an insulator region in contact with the p-well and between the p-type collector region and the heavily doped n-type emitter region; and

a gate electrode above the p-well, wherein the gate electrode is separated from the p-well by the insulator region.

12. The IC of Claim 11, wherein the second emitter electrode is connected to the p-well by at least one isolation structure, wherein each at least one isolation structure is a p-type structure.

13. The IC of Claim 12, wherein the at least one isolation structure includes a heavily doped p-type region in contact with the second emitter electrode.

14. The IC of Claim 13, wherein the heavily doped p-type region is located remotely from the heavily doped n-type emitter region, and

wherein the first emitter electrode is directly connected to the second emitter electrode.

15. The IC of Claim 11, wherein the first n-well comprises a heavily doped n-type punch through reduction region forming a first butting junction with the insulator region and a second butting junction with the p-type collector region.

16. The IC of Claim 11, wherein the first n-well comprises a heavily doped n-type buffer region that forms a butting junction with the insulator region, and wherein the p-type collector region is formed within the heavily doped n-type buffer region.

17. The IC of Claim 11, wherein the contact pad is connected to the gate electrode by a collector clamp, the collector clamp comprising one or more diodes.

18. The IC of Claim 11, wherein the transistor is formed on the contact pad.